O.P.Code: 20MC9101

R20

H.T.No.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR (AUTONOMOUS)

MCA I Year I Semester Regular & Supplementary Examinations January/ February-2025 COMPUTER ORGANIZATION

Time: 3 Hours		3 Hours	Max. Marks: 60		
(Answer all Five Units $5 \times 12 = 60$ Marks)					
		UNIT-I			
1		Convert the following:	CO 1	L3	12M
		i). (1011001) ₂ =(?) ₁₀			
		ii). (160) ₁₀ =(?) ₂			
		iii). $(2980)_{10} = (?)_8$			
		iv). (10110001101011) ₂ =(?) ₁₆			
		v). (3971) ₁₀ =(?) ₁₆			
		vi). (306.D) ₁₆ =(?) ₂			
		OR			
2		Illustrate the Encoder in detail with Truth Table.	CO1	L2	6 M
	b	Illustrate the Decoder in detail with Truth table.	CO ₁	L2	6M
		UNIT-II			
3		Discuss about the cache memory in detail.	CO ₂	L3	6M
	b	Differentiate the types of mappings.	CO ₂	L3	6M
		OR			
4		Discuss about Logic Micro Operations with neat representations.	CO ₂	L3	12M
		UNIT-III			
5		Explain about assembler directives.	CO ₃	L2	6M
	b	Explain about Data transfer instructions.	CO ₃	L2	6M
		OR			
6		Explain about Programming with assembly language instructions with	CO ₃	L2	12M
		example.			
		UNIT-IV		_	
7		Compare memory mapped I/O and isolated I/O.	CO4	L4	6M
	b	Compare I/O and Memory bus	CO4	L4	6M
_		OR	604		<i>(</i> 3.7
8		Discuss the Programmed I/O in detail.	CO4	L2	6M
	b	Explain about Interrupt-initiated I/O in detail.	CO4	L2	6 M
_		UNIT-V	CO.		<i>(</i>) <i>(</i>
9		Explain about Parallel Processing and its Types?	CO5	L2	6M
	b	Design the concept of Pipelining with clear example with neat sketch?	CO ₅	L3	6 M
10		OR	COS	т 2	1984
10		Discriminate about Inter Process Communication and Synchronization	CO5	L3	12M
		in detail.			